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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,492	03/01/2004	Nobuaki Hashimoto	118876	9029

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EXAMINER	
RICHARDS, N DREW	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,492	HASHIMOTO, NOBUAKI	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 8, 11, 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 01-164044 (cited in IDS filed 9/28/05) in view of Ling et al. (USPAT 6,445,069 B1).

With regard to claim 1, JP 01-164044 teaches an electronic device in figure 3 comprising:

- a substrate 1 on which an interconnect pattern 2 is formed;
- a chip component 4 having a base material and having a first surface (top surface) and a second surface (bottom surface) opposite to the first surface, the chip component 4 being mounted in such a manner that the second surface faces the substrate 1;
- a metal layer 4a formed on the first surface of the chip component;
- an insulating section 6 formed adjacent to the chip component 4; and
- an interconnect 7 which is formed to extend from above the top of the metal layer 4a, over the insulating section 6 and to above the interconnect pattern 2.

JP 01-164044 does not explicitly teach a pad formed on the first surface and a metal layer formed of a plurality of layers including a diffusion prevention layer in

contact with the pad and an uppermost layer being less oxidizable than the pad, the diffusion preventing layer preventing any diffusion of material formed thereabove into the base material of the chip component. JP 01-164044 does teach a less oxidizable uppermost layer of a noble metal such as gold. Though JP 01-164044 uses the term "electrode land part" for where the gold is formed, one of ordinary skill in the art would recognize that an "electrode land part" is the same as a "pad" as claimed since the land part of JP 01-164044 clearly refers to the portion where external electrical connections 7 are made to the chip.

Ling et al. teach a chip component 10 of a base material having a first surface on which a pad 26 is formed and metal layer 32/34/36 formed of a plurality of layers including a diffusion prevention layer 32/34 in contact with the pad and an uppermost layer 36 being less oxidizable than the pad, the diffusion prevention layer preventing any diffusion of material formed thereabove into the base material of the chip component.

JP 01-164044 and Ling et al. are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the metal layer 32/34/36 of a plurality of layers by the method taught by Ling et al. on the "electrode land part" or pad portion of layer 4a of JP 01-164044. The motivation for doing so is to allow the use of copper interconnect metallization while facilitating the electrical coupling of connection pads to supporting substrates or other packaging while using known metal deposition processes in a simple and inexpensive manner that is compatible with gold bond wires, solder bumps, and other common circuit connection

methods and that allows tight spacings between adjacent connections pads without compromising the reliability of the integrated circuit.

With regard to claim 2, the insulating section is formed of resin.

With regard to claims 3 and 4, the insulating section has an inclined surface descending in an outward direction from the chip component.

With regard to claim 5, JP 01-164044 as combined with Ling et al. above perform the claimed "mounting" and "forming" steps as claimed to arrive at the same device of claim 1.

With regard to claim 8, the insulating section is formed of resin.

With regard to claims 11 and 14, the insulating section has an inclined surface descending in an outward direction from the chip component.

With regard to claim 17, JP 01-164044 teaches a circuit board 1 on which the device of claim 1 is mounted. For arguments sake, if claim 17 requires a further circuit board on which the device including substrate 1 of JP 01-164044 is mounted, this claim is still considered obvious as it would have been obvious to one of ordinary skill in the art at the time of the invention to mount the device of JP 01-164044 on a printed circuit board in order to integrate the devices formed therein with other devices, such as mounting the chip on the mother board of a computer.

With regard to claim 18, the device of JP 01-164044 is considered an electronic instrument.

3. Claims 6, 7, 9, 10, 12, 13, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 01-164044 with Ling et al. as applied to claims 1-5, 8, 11, 14, 17 and 18 above, and further in view of Ito et al. (US Patent No. 6,625,032 B1).

With regard to claims 6 and 7, JP 01-164044 does not explicitly teach the interconnect being formed of a dispersant including electrically conductive particles or forming the layer includes ejecting the material over the metal layer, the insulating section, and the interconnect pattern.

Ito et al. teach on column 1 lines 30-37 that a dispersant including electrically conductive particles is ejected onto a substrate to form conductive layers. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the prior art conductive particles in dispersant ejecting method of Ito et al. in the method of JP 01-164044 to obtain rapid implementation of interconnects on surfaces.

With regard to claims 9 and 10, JP 01-164044 teach the insulating section formed of resin.

With regard to claims 12, 13, 15 and 16, JP 01-164044 teach the insulating section has an inclined surface descending in an outward direction from the chip component.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent

and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-18 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-34 of copending Application No. 10/788449 in view of JP 01-164044 and Ling et al. Claims 1-34 contain all the limitations of claims 1-18 except for a metal layer on the pad where

the metal layer is a plurality of layers as claimed, and the insulating section having an inclined surface. However, the plurality of metal layers as claimed is obvious in view of Ling et al. for the same reasons as explained above. The insulating section having an inclined surface is obvious in view of JP 01-164044 which teaches an incline in the resin insulator to allow for a plane with no steep stepped part so that a low cost interconnection method such as screen printing can be used.

This is a provisional obviousness-type double patenting rejection.

Response to Arguments

6. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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